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AN 8X-REAL-TIME DIFAR MULTIPLEXER-DEMULTIPLEXER SYSTEM

BY ARTHUR DELAGRANGE

WEAPONS SYSTEMS DEPARTMENT

13 JULY 1993

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NAVAL SURFACE WARFARE CENTER
DAHLGREN DIVISION • WHITE OAK DETACHMENT
Silver Spring, Maryland 20903-5640

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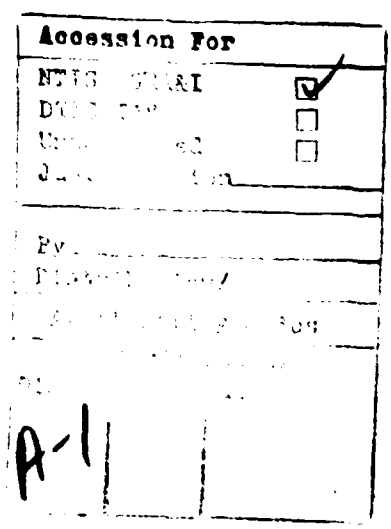
FOREWORD

DIFAR multiplexers and demultiplexers designed by the Center's U20 Division were described in detail in NAVSWC TR 91-334. This report describes the circuitry of an 8X-real-time version of the system developed for high-speed demultiplexing of tape-recorded data.

Approved by:

David S. Malyevac

DAVID S. MALYEVAC, Deputy Head
Weapons Systems Department



ABSTRACT

DIFAR multiplexers and demultiplexers designed by the Acoustic Signal Processing Branch, Naval Surface Warfare Center Dahlgren Division, have been described in a previous report. This report describes modifications to make the system work at 8X-real-time, primarily for high-speed demultiplexing of tape-recorded data.

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ILLUSTRATIONS

INTRODUCTION

DIFAR multiplexers and demultiplexers designed by the Acoustic Signal Processing Branch have been in use for a number of years. Recently a redesign was completed and a report published[1]. Concurrently a limited effort was made to make the circuitry operate eight times faster. This would speed the job of reducing volumes of taped multiplexed data to (taped) demultiplexed data.

The effort was partially successful. The system works, but dipole channel separation is only about 25 dB, vice 30 + dB for the normal system.

Theory and operation of the basic system is given in detail in Reference 1 and will not be repeated here, as it all applies here if the numbers are simply changed by a factor of eight. The new circuit diagrams are given, and the changes are described in the text.

CIRCUITRY

A ground rule was that the existing circuit boards had to be used with only slight modification. Thus, primarily, only components were changed, although a few topography changes were "hacked in" on the boards. Considerable care was necessary to make even the original boards work properly, as maintaining a fraction of a degree of phase accuracy at 15 kHz implies logic rise and delay times of less than 100 nsec, and maintaining gain accuracies better than 1% implies analog bandwidths of several megahertz. Readily available integrated circuits were adequate for the standard system, but not for the 8X faster system. In some cases high-speed versions of deficient circuits were not available.

Although the multiplexer input filters (Figure 1) operate linearly and pass only 40 kHz, they must reject higher frequencies properly without going nonlinear. Also, the "supercapacitor" circuits require considerable extra bandwidth as they are essentially part of tuned circuits. Substitution of newer, higher-speed quad op-amps in these gave a reasonable filter response. However, an unanswered question is: How much variation is to be expected between channels, as mismatch directly affects the amplitude accuracy of the signals.

Otherwise, the changes are simply changes in the values of the passive components to reflect the effectively 8X higher frequencies. This could have been done simply by reducing all capacitors by a factor of eight, but doing that would have given a

1 Delagrange, A. D., *DIFAR Multiplexer-demultiplexer System, Latest Improvements*, NAVSWC TR 91-344, 1 May 1992, Naval Surface Warfare Center, White Oak, Md.

nonstandard value not readily available; so instead the filter capacitors were reduced by a factor of ten and the resistors adjusted accordingly.

In the multiplexer output circuit (Figure 2), capacitors and inductors in the filter circuit were reduced by a factor of 10, leaving the impedance unchanged. This gives a cutoff frequency slightly higher than necessary, but this is not critical. The oscillator is now 480 kHz.

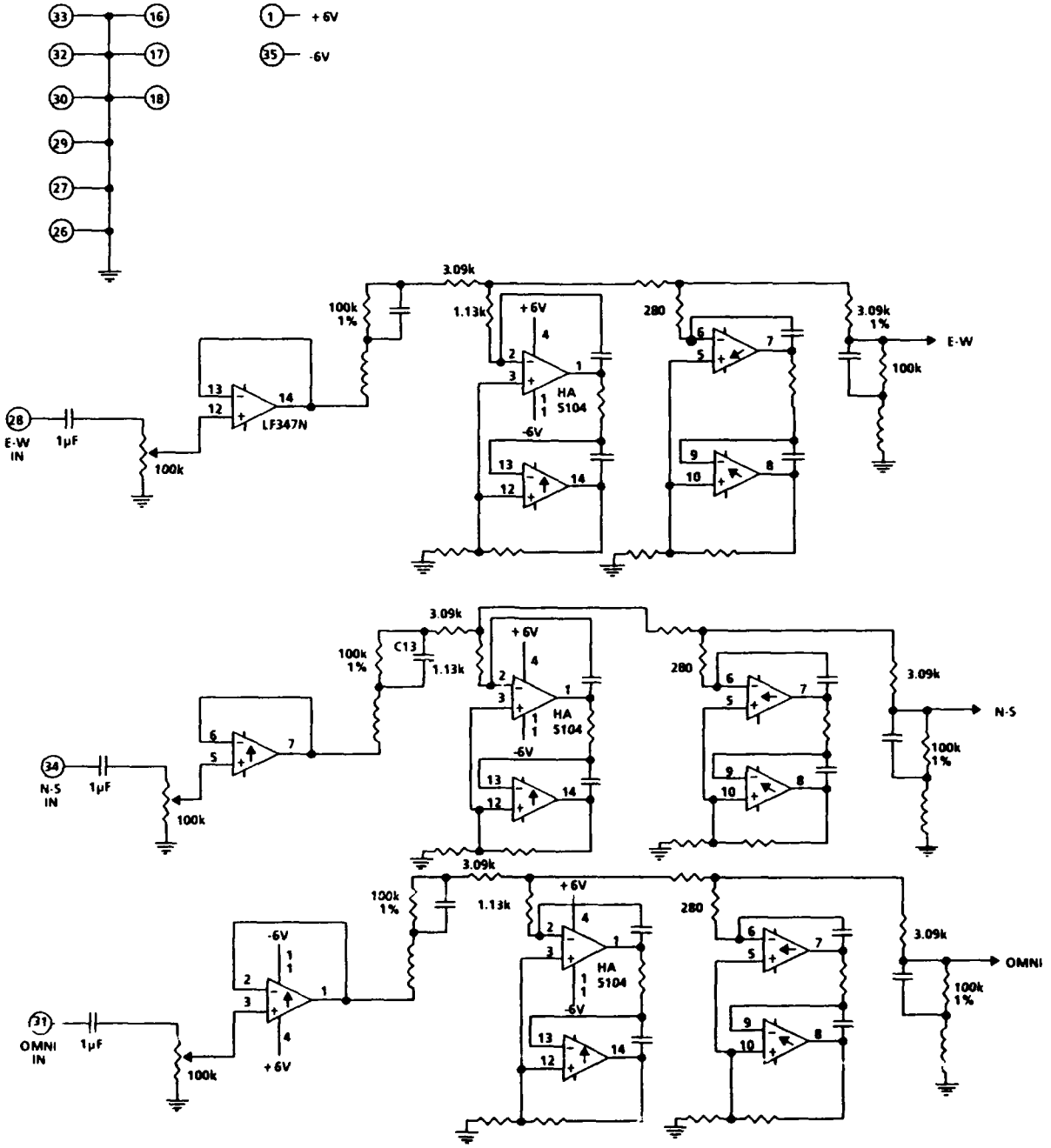
In the demultiplexer phase-lock loop (Figure 3), values in the integrators have been reduced to raise the loop speed by a factor of 10, reflecting the faster tape speed. In the 7.5-kHz (now 60-kHz) filter the capacitors have been reduced by a factor of 10 and the resistors adjusted accordingly. New high-speed op-amps are used. These have rather high input current, and the resulting offset required that the comparator following be AC-coupled. Also, the more expensive grade of comparator is now required to ensure adequate speed. The tuning inductor in the Voltage-Controlled Oscillator (VCO) is reduced by a factor of 10; the Voltage-Variable Capacitor (VVC) already was the lowest value of the series. Fortunately, these need not be exact, as the capacitor is automatically adjusted by the loop anyway.

The demultiplexer output filters (Figure 4) are the same as the multiplexer input filters already discussed, and the changes are identical.

CONCLUSION

Although theoretically all that is necessary to increase the speed (frequency) of the system is to reduce the values of the reactive components by a corresponding amount, in practice there is a number of problems as frequency is increased. The finite speed of the integrated circuits causes bigger relative errors. Stray capacitance becomes more significant. It is desirable to keep the reactive components at common values, so juggling the resistor values is necessary.

Only prototypes were built, and limited testing was done. Some of the niceties eventually added to the standard units are not included here, *e.g.*, overload indication for the multiplexer. Substantial improvements to the circuitry are probably possible only through improved integrated circuits not yet on the market, or larger circuit boards to allow major changes in circuit design. However, the circuits are quite usable in their present form, albeit at somewhat reduced accuracy.



NOTES:

UNMARKED RESISTORS	**6.19 kΩ 1%**
UNMARKED CAPACTORS	**1000 pF 1%**
UNMARKED INDUCTORS	**10 mH**

FIGURE 1. 8X-MULTIPLEXER INPUT FILTERS

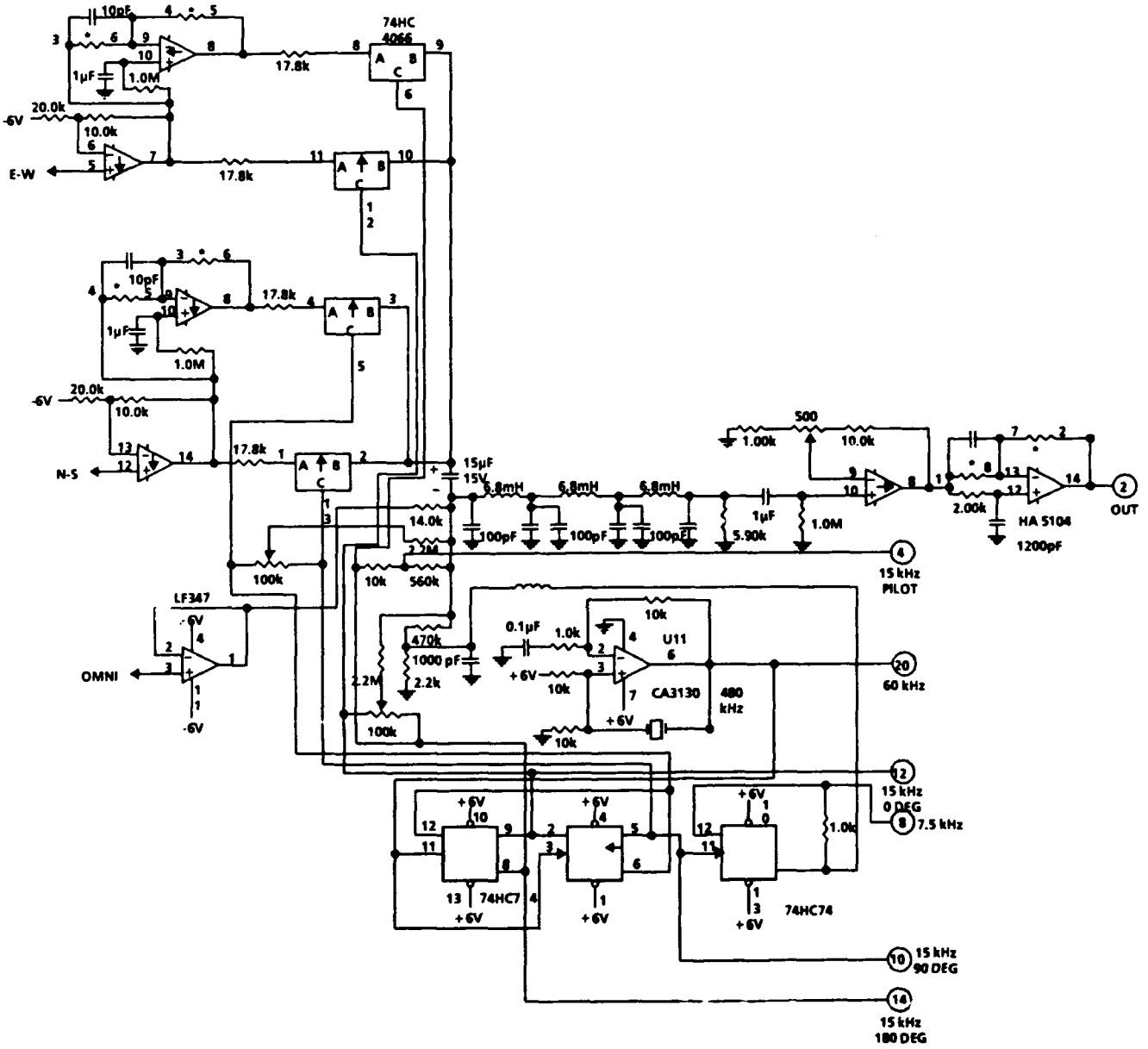


FIGURE 2. 8X-MULTIPLEXER SUMMING CIRCUIT

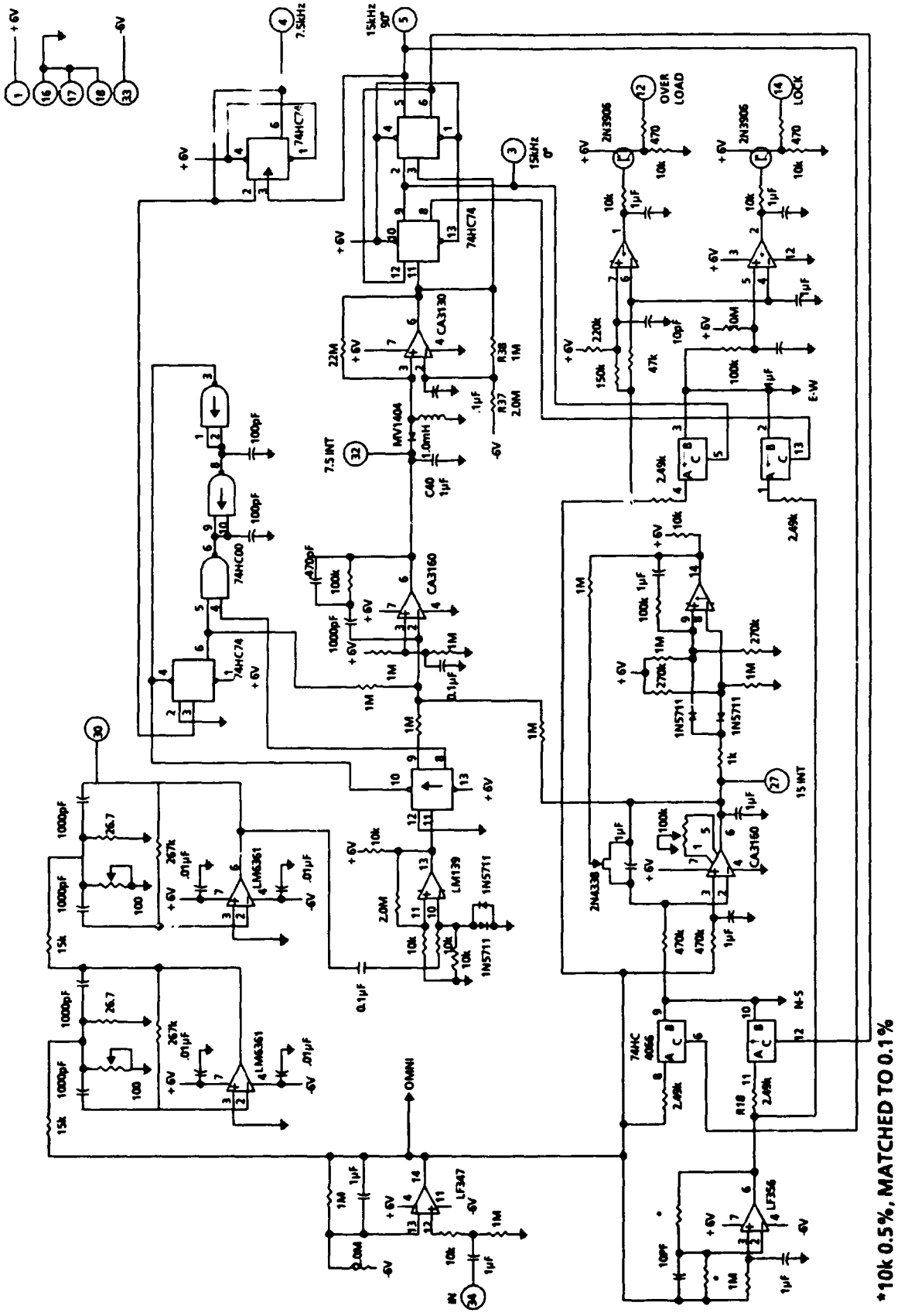
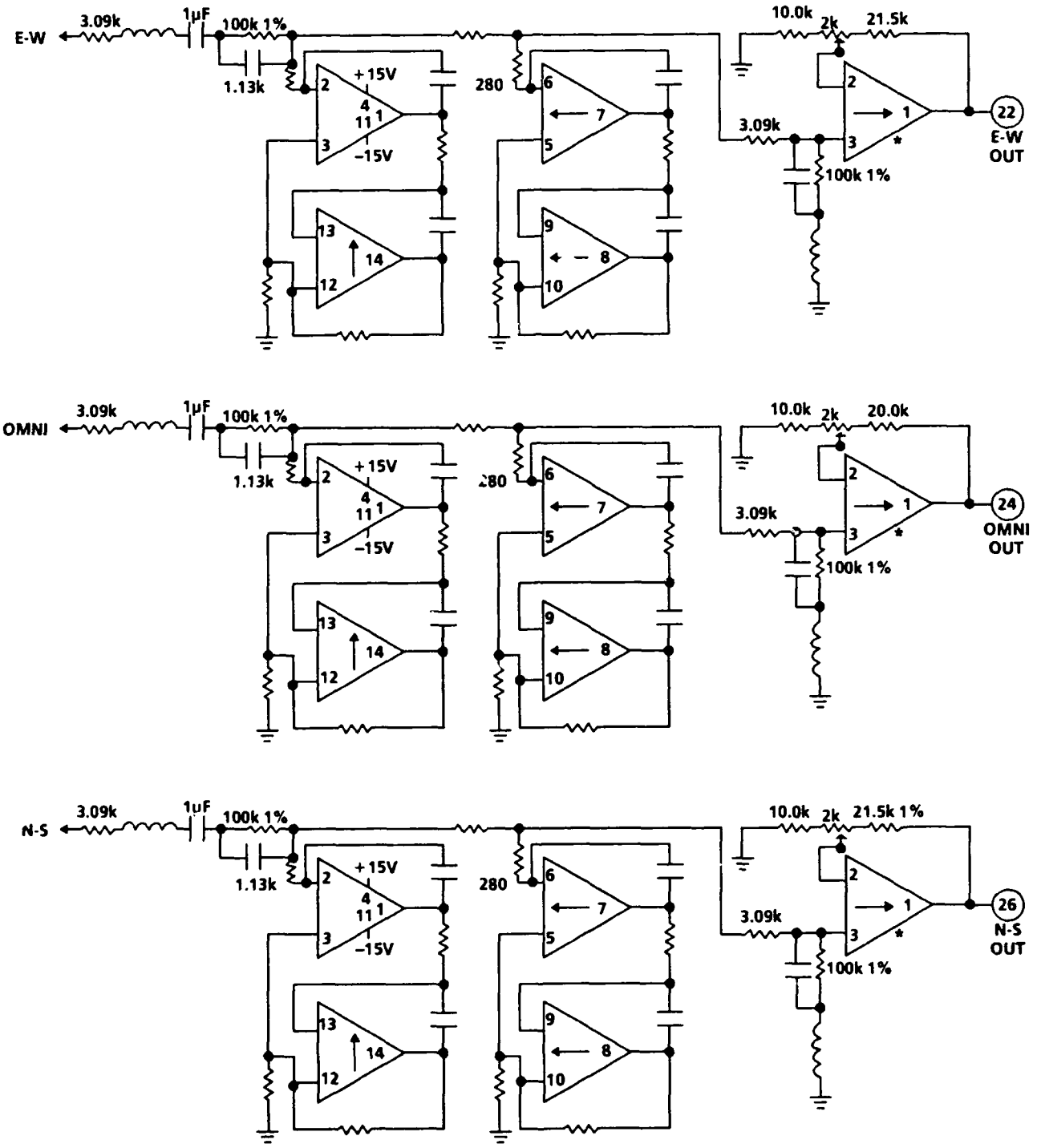


FIGURE 3. 8X-DEMULTIPLEXER PHASE-LOCK LOOP CIRCUIT



NOTES: UNMARKED CAPACITORS 1000pF 1%
UNMARKED RESISTORS 6.19k 1%
ALL INDUCTORS 10 mH
ALL OP AMPS HA 5104 EXCEPT * LF 347

FIGURE 4. 8X-DEMULTIPLEXER OUTPUT FILTER CIRCUITS

APPENDIX A

MULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±6V ±15 mV. If supplies cannot be adjusted, recalibrate card with the same supply it is operated with (step 3 primarily).

2. Check oscillator output (pin 20). It should be a square waveform, 0 to +6V, 480.000 kHz ±300 Hz.

3. Set the three inputs pots half way up. Observe the output (pin 2) with no signals in. Ground pins 4 and 8. Adjust the two balance pots alternately for minimum output signal using a filter set at 120 kHz and a true-RMS AC voltmeter, or spectrum analyzer observing the 120-kHz line.

4. Ground pin 8 only. Output should be 120 kHz ±120 Hz, fairly sinusoidal. Adjust output pot for 100 mVRMS (-20dBV).

5. Ground pin 4 only. Output should be 60 kHz ±60 Hz, sinusoidal. Amplitude should be about 100 mVRMS. There is no adjustment.

6. Ground pins 4 and 8. Place a 10-kHz, 1-VRMS sine on OMNI in (pin 31). Adjust the corresponding input pot for 0.707 VRMS (-3dBV) at output. Repeat for E-W in (pin 28). On a spectrum analyzer this will be -6dBV lines at 110 kHz and 130 kHz. Repeat for N-S in (pin 34). Place signal on all three inputs. Overload lamp should light.

7. Check frequency response. For each of the three channels, increase input frequency until output level drops 3 dB from that at 10 kHz. Input frequency should be 40 kHz ±4 kHz.

8. As a double check, connect the multiplexer to a demultiplexer if available (this step is optional but it may show up problems the calibration procedure does not catch). Place a 10-kHz 1-VRMS (0 dBV) sine wave on the N-S input. Lock lamp should be lit. Overload lamp should be dark. Check to see that the 10-kHz 1-VRMS input signal appears at the N-S output. Move input signal to E-W input and check to see that it appears at the E-W output. Move signal input to OMNI to see that it appears at OMNI output. Output level should be 0 dBV ±0.3 dB for all three cases. Signal on the two unused channels should be below -25 dBV in all cases. Check frequency response for all three channels. It should be down 6 dB at 40 kHz ±4 kHz. On the low end it should drop less than 3 dB at 25 Hz. Check feedthrough and noise at the outputs with no signals in. It should be below -50 dBV for each, true RMS.

APPENDIX B

DEMULTIPLEXER CHECKOUT AND ADJUSTMENT

1. Insert card into rack or test fixture. Make sure supplies are adjusted to ±6V ±15 mV. If supplies cannot be adjusted, card should be readjusted with the same supply it is operated with (step 3 primarily).

2. Place a 60-kHz, 100-mV RMS (-20dBV) sine wave on the input (pin 34). Adjust the pots for 180-degree phase shift through each section. Recheck filter to see that it peaks at 60 kHz ±600 Hz.

3. Place a 200-kHz, 1-VRMS (0dBV) sine wave on the input (pin 34). Set the 120-kHz integrator balance pot fully counterclockwise. The output (pin 27) should drift up to about 4.5 V, reset to about +3 V, drift up again, etc. Set the pot fully clockwise. The output should drift down to about 1.5 V, reset to about +3 V, drift down again, etc. Adjust the pot for minimum drift of the 120-kHz integrator by observing the voltage at pin 27 with a voltmeter having at least 1-mV sensitivity.

4. Change input to 10 kHz. Adjust the OMNI pot for 1.4 VRMS (+3 dBV) at OMNI output (pin 24). Lock lamp should not light.

5. Place at the input a composite waveform consisting of a 130-kHz, 0.5-VRMS (-6 dBV) sine wave plus a 60-kHz, 0.5-VRMS (-6 dBV) rectangular wave of 75%, 25% duty cycle. Lock lamp should light. Overload lamp should not light. N-S (pin 26) and E-W (pin 22) outputs should be sine waves, 10 kHz. Adjust the dipole pots to give 0.5 VRMS (-6 dBV) at each. Increase the sine wave amplitude 10 dB. Overload lamp should come on.

6. Check the frequency response of the OMNI by inserting the signal of step 4 but increasing the frequency until the OMNI output amplitude drops 3 dB. Frequency should be 40 kHz ±4 kHz. Check the frequency response of each dipole by inserting the composite signal of step 5 but increasing the input sine wave frequency until the output amplitude drops 3 dB. Output frequency should be 40 kHz ±4 kHz. Check feedthrough and noise by observing the three outputs with no signal into the demultiplexer. It should be below -40 dBV for each, true RMS.

7. As a double check, connect a multiplexer to the demultiplexer if available (this step is optional but it may show up problems the calibration procedure does not catch). Place a 10-kHz, 1-VRMS (0 dBV) sine wave on the N-S input. Lock lamp should light. Overload lamp should not light. Check to see that the 10-kHz, 1-VRMS input signal appears at the N-S output. Move the input signal to the E-W input and check to see that it appears at the E-W output. Move the input signal to OMNI input and check to see that it appears at the OMNI output. Output level should be 0 dBV ±0.3 dB for all three cases. The signal on the two unused channels should be below -25 dBV in all cases. Check the frequency response for all three channels. It should be down 6 dB at 40 kHz ±4 kHz. Check feedthrough and noise at the outputs with no signals in. It should be below -50 dBV for each, true RMS.

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DIFAR multiplexers and demultiplexers designed by the Acoustic Signal Processing Branch, Naval Surface Warfare Center Dahlgren Division, have been described in a previous report. This report describes modifications to make the system work at 8X-real time, primarily for high-speed demultiplexing of tape-recorded data.

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